

Influence of channel length and layout on TID for 0.18 μm NMOS transistors

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Abstract Different channel lengths and layouts on 0.18 μm NMOS transistors are designed for investigating the dependence of short channel effects (SCEs) on the width of shallow trench isolation (STI) devices and designing in radiation hardness. Results show that, prior to irradiation, the devices exhibited near-ideal I - V characteristics, with no significant SCEs. Following irradiation, no noticeable shift of threshold voltage is observed, radiation-induced edge-leakage current, however, exhibits significant sensitivity on TID. Moreover, radiation-enhanced drain induced barrier lowering (DIBL) and channel length modulation (CLM) effects are observed on short-channel NMOS transistors. Comparing to stripe-gate layout, enclosed-gate layout has excellent radiation tolerance.

Key words SCEs, DIBL, CLM, Enclosed-layout

1 Introduction

The incredibly rapid growth in the performance and throughput of MOS process over last thirty years has led to a microelectronics revolution that has profoundly changed the world. Continued improvement in the performance of commercial and space satellite systems will depend critically on the rate of insertion of advanced MOS process and microelectronics technologies into these systems. Process scaling can be defined as reducing the sizes thickness of gate oxide and the classic LOCOS-based isolation is abandoned for shallow trench isolation (STI), allowing a further reduction of the device pitch. In modern submicron and deep submicron bulk MOS technologies, the radiation induced gate threshold voltage shift and gate oxide leakage current are not major factor limiting total dose hardness, radiation-induced leakage current in the isolation oxide, however, is becoming the most common problem^[1-3]. Following devices size scaling, the length

of depletion of source and drain is analogous to channel length, so some effects which ignored in large size MOS transistors become important, such as channel length modulation effects, and drain induced barrier lowering effects as a result of channel length scaling. That is why it is necessary that we should make some research about these effects. Radiation enhanced SCEs, DIBL effects on 0.6 μm MOS transistors had been reported by Luo Yihong and co-workers in 2010^[4]. G.U. Youk and his work-fellows reported radiation enhanced SCEs on devices with 0.35 μm and 0.4 μm channel length^[5]. The influence of channel length on total ionizing dose effect in 0.18 μm NMOS transistors have been reported by Hu Zhiyuan and his colleagues^[6,7]. In this contribution, we design devices with different W/L sizes and gate layouts for radiation-enhanced SCEs and radiation tolerance on stripe gate and enclosed gate.

2 Experimental details

The NMOS transistors studied in this work belong to

Supported by National Laboratory Analog Integrated Circuit Foundation(No. 9140C090402110C0906)

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Received date: 2013-01-18

the 0.18 μm CMOS process with STI. The oxide thickness is 3.981 nm. Test chips were designed and fabricated, including stripe gate layout with L of 20 μm , 1.2 μm , 0.5 μm , 0.18 μm and W of 20 μm and enclosed gate layout with L of 1.2, 0.18 μm and W of 20 μm . The operating voltage is 1.8V. The devices were irradiated in a ^{60}Co gamma irradiation chamber at the Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences. During exposure, the gates of the samples were biased at 1.8V and all other pins grounded. I - V characteristics measurements were obtained prior to irradiation and after step stress irradiation up to 100 krad(Si), 200 krad (Si), 300 krad(Si), and 500 krad(Si). These measurements were taken within 20 min exposure.

3 Results and discussion

According to literature, the susceptibility on gate oxide is reduced following its thickness scaling, therefore, shift on threshold voltage has not been a problem. Although STI is becoming the dominant isolation technology for advanced CMOS processes, it is still sensitive on TID.

A. Radiation-induced leakage

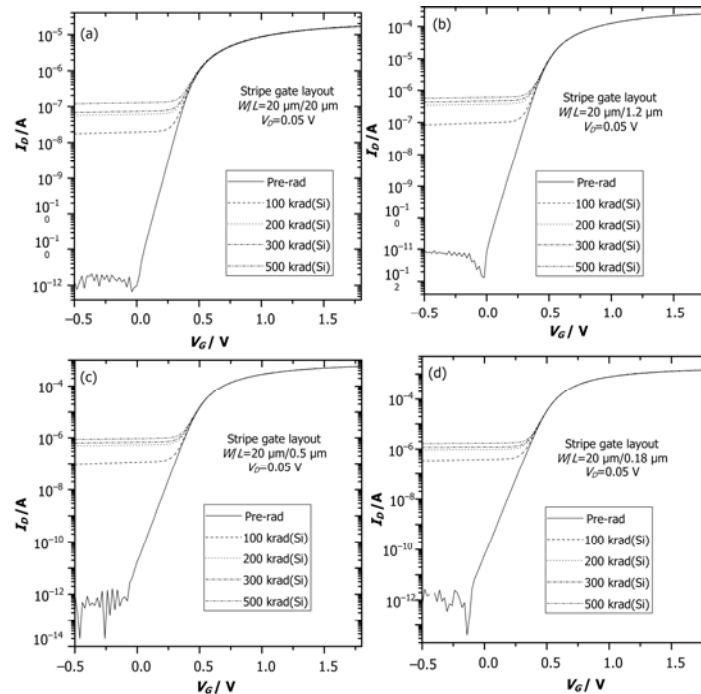


Fig.1 Relationship between I_D - V_G characteristics and total dose for transistors with (a) $W/L = 20 \mu\text{m}/20 \mu\text{m}$, (b) $W/L = 20 \mu\text{m}/1.2 \mu\text{m}$, (c) $W/L = 20 \mu\text{m}/0.5 \mu\text{m}$, (d) $W/L = 20 \mu\text{m}/0.18 \mu\text{m}$.

B. Radiation enhanced channel length modulation

Fig.2 shows the I_D - V_D characteristic of parasitic

The test transistors were irradiated up to a total dose of 500 krad (Si). Fig.1 shows the I_D - V_G characteristics for devices with different channel lengths. As can be seen from Fig.1, the curves obtained after a total dose of 100 krad (Si) exhibit pronounced subthreshold leakage. When the total ionizing dose accumulated to 500 krad (Si) the drain current at $V_G=0$ V is approximately 5 orders of magnitude higher than the corresponding pre-irradiation value. The radiation-induced excess leakage current shows weak gate control, which means the leakage current is mainly due to the parasitic transistors along the trench oxides^[7,8]. As we all know, the positive charge trapped in the lateral STI oxide can be enough to invert the channel and open a conductive channel through which leakage current can flow between source and drain and the parasitic transistors turn on. As the total dose increased, more oxide trapped charges are built up in the STI oxide, which enhanced the leakage current. Since this leakage current is small compared to the current that flows in the main transistor, it influences the subthreshold region of the transistor I_D - V_G curve but not the region above threshold, as shown in Fig.1.

transistors with stripe gate layout. From Fig.2, we can see that noticeable radiation-induced channel-length

modulation (CLM) effect was observed up to 500 krad (Si) with L is 20 μm while up to 100 krad (Si) with L is 0.18 μm , exhibiting radiation-enhanced CLM effects. So we have, in saturation^[9],

$$I_D \approx \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_G - V_T)^2 (1 + \lambda V_D) \quad (1)$$

where μ_n is electron mobility, C_{OX} is unit area of

gate oxide capacitance, W is gate width, L is channel length, V_G is gate voltage, V_T is threshold voltage, V_D is drain voltage, and λ ($\lambda = ((1 - L_{\text{eff}})/L)/V_D$) is the channel-length modulation coefficient. This phenomenon results in a nonzero slope in the I_D - V_D characteristic and hence a nonideal current source between drain and source in saturation.

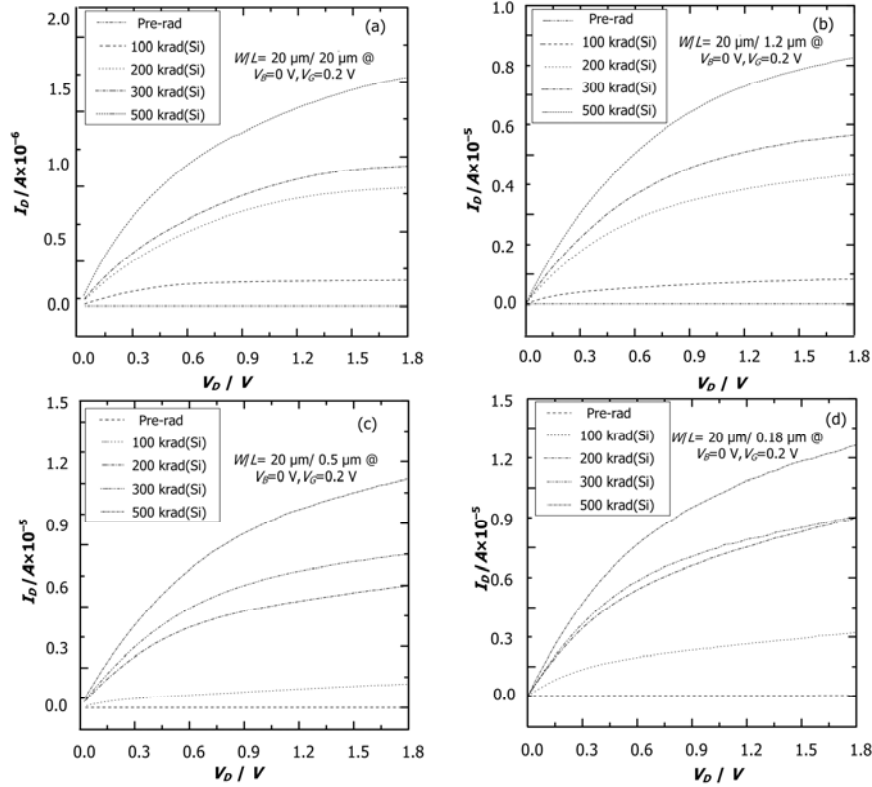


Fig.2 I_D - V_G characteristics as a function of total dose for parasitic transistors with (a) $W/L = 20 \mu\text{m}/20 \mu\text{m}$, (b) $W/L = 20 \mu\text{m}/1.2 \mu\text{m}$, (c) $W/L = 20 \mu\text{m}/0.5 \mu\text{m}$, (d) $W/L = 20 \mu\text{m}/0.18 \mu\text{m}$.

From Fig.3, we can see that following irradiation, the slope in the I_D - V_D characteristic of parasitic transistors increases. We can see that the smaller the L , the more serious the slope is. As previously mentioned, radiation-induced leakage current only had influenced the subthreshold region of the main transistor, which is related with the parasitic transistors. That is the reason for the changes of slope. As we all know, the point at which the local density of inversion layer charge equals zero gradually moves toward the source as V_D increases. We assume that the $L_{\text{eff}} = L$ when $V_D = V_G - V_T$, so the L_{eff} is eliminated as V_D increases, i.e., the L_{eff} is eliminated as V_T decreases.

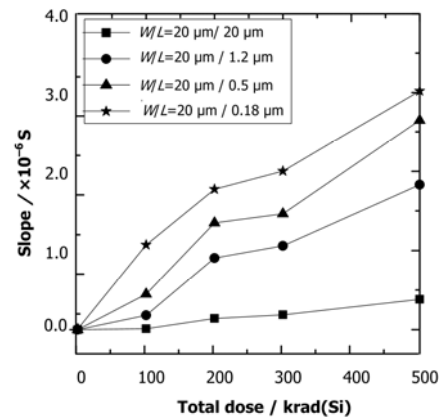


Fig.3 Slope in the I_D - V_D characteristic as a function of total dose for parasitic transistors.

Prior to irradiation, the threshold voltages of parasitic transistors are large enough for keeping them off. Following irradiation, positive charges are trapped in the lateral STI oxide and come into being oxide trapped charges. These charges result in a negative shift of V_T of parasitic transistors and that result in the eliminating of L_{eff} eventually. The shorter the L is, the more serious the CLM effects are. This phenomenon was found only on parasitic transistors, which will not influence the L of main transistors, so we do not need to consider much more about it on analog integrated circuits where the transistors is always in saturation region.

C. Effects of drain bias during measurement

For short channel NMOS transistors, punchthrough which caused by drain induced barrier

lowering (DIBL) will happen at the surface or in the bulk. At the trench oxides, radiation-induced charge can escalate devices punchthrough in three different ways^[5]. Fig.4 illustrates the pre- and post-irradiation I_D - V_G characteristics with devices $W/L = 20 \mu\text{m} / 20 \mu\text{m}$, $W/L = 20 \mu\text{m} / 1.2 \mu\text{m}$, $W/L = 20 \mu\text{m} / 0.5 \mu\text{m}$, $W/L = 20 \mu\text{m} / 0.18 \mu\text{m}$ at different drain biases. As channel length shortens, the pre-irradiation current-voltage curves show slightly DIBL effects at subthreshold region while exhibits significant DIBL effects at saturation region. Following irradiation, according to (a), (b), (c) and (d), the subthreshold regions of the transistors exhibit substantial radiation-induced DIBL effects. This can be explained by charge sharing with the source and the drain junctions.

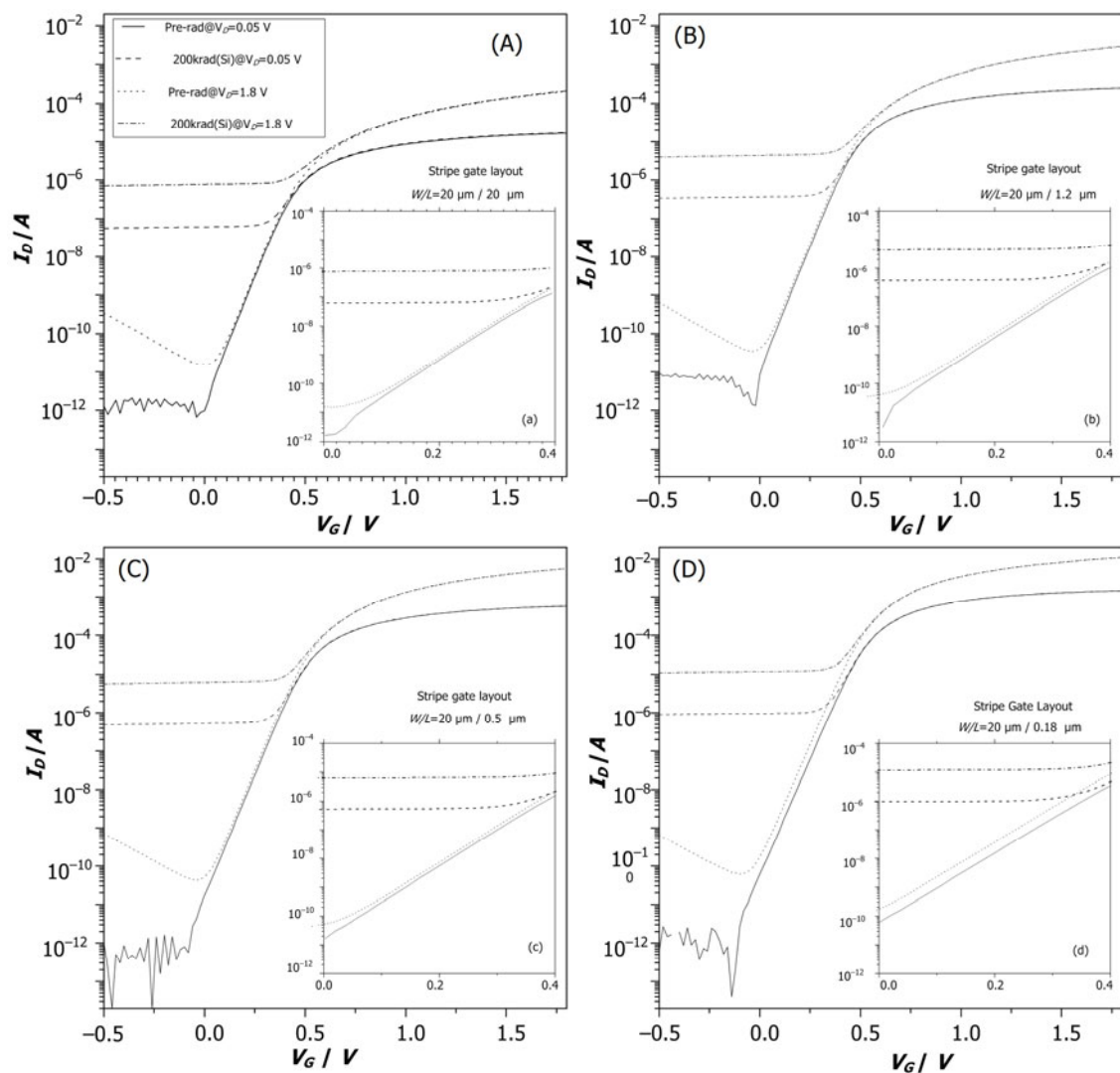


Fig.4 I_D - V_G characteristics for transistors at different drain biases. (A) $W/L = 20 \mu\text{m} / 20 \mu\text{m}$, (B) $W/L = 20 \mu\text{m} / 1.2 \mu\text{m}$, (C) $W/L = 20 \mu\text{m} / 0.5 \mu\text{m}$, (D) $W/L = 20 \mu\text{m} / 0.18 \mu\text{m}$. (a), (b), (c) and (d) subthreshold regions of these transistors.

On one hand, irradiation-induced positive oxide charges are quickly trapped in the STI oxide at the transistor edge. These charges raise the nearby body potential, lowering potential barrier with the drain and the source, resulting in bulk punchthrough. On the other hand, the positive charge trapped in the lateral STI oxide accumulate, and eventually builds up a depletion region along the trench oxides, called parasitic depletion regions. The parasitic depletion region shortens the effective channel length through interactions with the drain and source depletion region and meets with the drain depletion region and with the source depletion region around the corner, thus enhancing the DIBL effects^[5,10].

D. Stripe-gate and Enclosed-gate layout versus TID

As discussed in part A, the effect of total-dose irradiation on isolation, standard-edged NMOS transistors is to cause an increase in the off-state leakage current. This increased leakage current is caused by the inversion of parasitic transistors at the

transistors edges at or near the gate oxide/isolation oxide interface. We design devices with enclosed-gate layout for eliminating the leakage current. This layout design technique which has no active diffusion edges overlapped by polysilicon that separate the source and the drain can eliminate edge leakage by removing the parasitic transistors between drain and source. It is precisely because of there are no active diffusion edges and parasitic transistors in the enclosed-gate layout, no radiation-induced leakage current was observed.

As seen in Fig.5, comparing to stripe-gate layout transistors, almost no irradiation-induced leakage current was observed on enclosed-gate layout transistors after a total dose of 500 krad (Si). About TID of the enclosed-gate layout, literature^[4] has done some work on bulk silicon 0.6 μm NMOS devices, results showed it had excellent radiation tolerance. Our work proved that this method was efficacious on 0.18 μm NMOS transistors further.

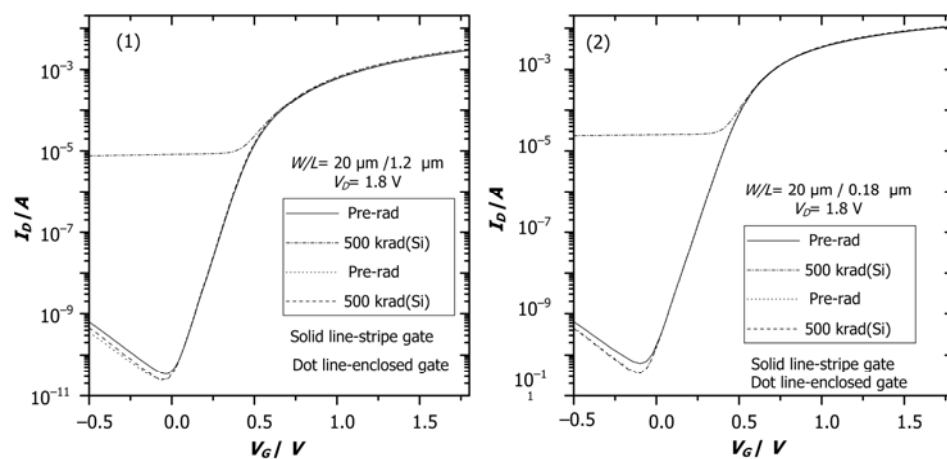


Fig.5 I_D - V_G characteristics for enclosed-gate layout transistors: (1) $W/L = 20 \mu\text{m} / 1.2 \mu\text{m}$, (2) $W/L = 20 \mu\text{m} / 0.18 \mu\text{m}$.

4 Conclusion

The study of the TID response of transistors with different gate lengths and layouts in a 0.18 μm commercial CMOS technology has shown radiation enhanced CLM and DIBL effects which are mainly due to the parasitic transistors characteristic degradation. The subthreshold region is more sensitive than saturation region when exposed to Gamma ray irradiation, so we should consider much more about that in digital integrated circuits than analog integrated circuits. The slope of I_D - V_D characteristic of the parasitic transistors continuously increases as total

ionizing dose increases, a typical channel length modulation effect. The slope is approximately 3 orders of magnitude higher than the corresponding pre-irradiation value for a gate length of 0.18 μm , and much more for normal length device (20 μm). Enhanced DIBL is attributed to (1) the raising the nearby body potential, lowering potential barrier with the drain and the source; (2) interaction between parasitic depletion region and the drain and source depletion region. The enclosed-gate layout has excellent radiation tolerance by removing the parasitic transistors between drain and source.

References

1. Lacoer C, Osborn J V, Koga R. *et al.* IEEE Trans Nucl Sci, 2000, **47**: 2334–2341.
2. Anelli G, Campbell M, Dachs C, *et al.* Proc. 3rd Workshop on Elec. for LHC Experiments, Sep. 1997, 139–143.
3. Manghisoni M, Ratti L, Re V, *et al.* IEEE Trans Nucl Sci, 2003, **50**: 1827–1833.
4. Luo Y H, Guo H G, Zhang F Q, *et al.* Research Progressofsse, 2010, **30**: 37–43.
5. Youk G U, Khare P S, Schrimpf R D, *et al.* IEEE Trans. Nucl Sci, 1999, **46**: 1830–1836.
6. Liu Z L, Hu Z Y, Zhang Z X, *et al.* J Soc, 2011, **32**: 064004(1–5).
7. Hu Z Y, Liu Z L, Shao H, *et al.* Acta Phys Sin, 2012, **61**: 050702.
8. Federico F, Giovanni C. IEEE Trans Nucl Sci, 2005, **52**: 2413–2417.
9. Behzad R. Design of Analog CMOS integrated circuits. 10#, Xingqing South Road, Xi An City, China (Xi An): Xian Jiao Tong University, Press, 2009, 9.
10. Liu Z L, Hu Z Y, Zhan Z X, *et al.* IEEE Trans Nucl Sci, 2011, **58**: 1324–1331.